Postdoc: Design and validation of a timing-predictable RISC-V-based multicore processor

TRACES group (IRIT lab)

One of the objectives of the ANR ASTRID PRINTEmPS project led by Thales and IRIT research lab is to design a time-predictable multicore processor, i.e. one for which precise upper bounds on *worst-case response time* (WCRT) can be derived for time-critical software tasks.

Introduction

Critical embedded systems are subject to time guarantee requirements, while at the same time requiring ever greater computing power, which can only be provided by multi-core processors. Off-the-shelf processors meet this need for performance but do not provide the safety guarantees, partly because the details of their internal architectures are not known, which prevents any reliable analysis of their behaviour, and partly because they were not necessarily designed for this purpose. The aim of the PRINTEmPS project is to propose a multicore processor that meets these safety requirements. The design of a specific processor enabled by the technological, software and organisational infrastructure of the RISC-V world guarantees complete control of the hardware architecture. This expertise will enable the relevant implementation of formal verification tools for the expected properties in terms of temporal behaviour.

The starting point of this project is MINOTAuR, a RISC-V execution core derived from the CVA6 core [1, 2, 3]. This core has an interesting property : the absence of temporal anomalies [5], which allows compositional analysis [4] on the scale of a multicore. This property has been formally proven on the basis of a logic model and using the Coq proof assistant.

Existing interconnect structures do not allow accurate analysis of the impact of interference on response times. The design of a formally proven predictable structure will be a major step forward for the deployment of critical applications on multicore architectures. The interface between a computing core and this interconnection structure should be carefully designed so as not to call into question the predictability of the core itself.

A second phase will involve calculating guaranteed limits for communication times. These delays can then be taken into account as part of a response time analysis.

Description of the position

The objective of the postdoc is to design the hardware of a multicore architecture based on MINOTAuR and to assess its time-predictability. More precisely, the postdoctoral researcher will :

— design a time-predictable interconnect structure between cores and shared memory,
— develop an interference analysis based on this interconnect,
— propose a WCRT analysis for tasks running in parallel on the multicore.

We aim for publications in top-tier conferences and journals from the real-time and computer architecture communities.

The postdoc will be located at IRIT. The position is for 18 months.

Skills

On top of holding a PhD in computer science or engineering, the applicant must master the following skills :

— Computer architecture
— SystemVerilog or VHDL Programming
— FPGA synthesis
— Scientific paper writing

As the position concerns a ZRR (Zone à Régime Restrictif) area, acceptance will require clearance from the Haut Fonctionnaire de Sécurité et de Défense.

Contacts

To apply, send a CV and motivation letter to :
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Références

[1] A. Gruin, T. Carle, H. Cassé, and C. Rochange. Speculative execution and timing predictability in an open source RISC-V core. In *IEEE Real-Time Systems Symposium (RTSS)*, pages 393–404, 2021.

[2] A. Gruin, T. Carle, C. Rochange, H. Cassé, and P. Sainrat. MINOTAuR : A timing predictable RISC-V core featuring speculative execution. *IEEE Transactions on Computers*, 72(1) :183–195, 2022.

[3] A. Gruin, T. Carle, C. Rochange, and P. Sainrat. Enabling timing predictability in the presence of store buffers. In *31st International Conference on Real-Time Networks and Systems, RTNS 2023*, 2023.

[4] Sebastian Hahn, Jan Reineke, and Reinhard Wilhelm. Towards compositionality in execution time analysis : definition and challenges. *SIGBED Review*, 12(1) :28–36, 2015.

[5] Jan Reineke, Björn Wachter, Stefan Thesing, Reinhard Wilhelm, Ilia Polian, Jochen Eisinger, and Bernd Becker. http ://drops.dagstuhl.de/opus/volltexte/2006/671A definition and classification of timing anomalies. In *International Workshop on Worst-Case Execution Time Analysis*, 2006.