Programme du colloque GdR SoC

Quelques informations complémentaires:

- Le créneau du Mardi 08 Juin est en distanciel
- Les créneaux du 09 et 10 sont en présentiel et distanciel
- Le distanciel se fera par Webinaire Zoom (info ci-dessous)
- Cliquez sur les noms des orateurs pour obtenir plus d'informations !
- La **session poster** distancielle se fait par le site Wonder.me (https://www.wonder.me/) et plus d'informations ici (https://hackmd.io/eUZ50u-lRISJcqAvAAjhow)
- Plus d'informations sur les **sessions poster** en présentiel ici (https://hackmd.io/NcX0rzVuTP6bWSfzukzjQQ) !

> Un pont Zoom unique sera utilisé pour l'ensemble des sessions pleinières en distanciel
>
> ➡️ Le pont Zoom (https://insa-toulouse-fr.zoom.us/j/94574152510?pwd=WU9KWFprMjlJOUJNYzRoMW1lVXkyZz09) ⬅️
>
> - Meeting ID: 945 7415 2510
> - Passcode: 585175

Journée du Mardi 08 Juin 2021

Tout en distanciel, Webinaire Zoom

Heures	Programme
08h45 - 09h30	Ouverture, Informations générales sur l'organisation du colloque
09h30 - 10h30	Session **"Sustainable SoC"** **Organisateurs**: Nathalie D, Abdoulaye G, Andréa P **Orateurs**: Vincent Courboulay puis Caroline Vateau
10h30 - 11h30	Session **"Calcul embarqué haute performance"** **Organisateurs**: Sebastien F, Abdoulaye G **Orateurs**: Steven Derrien puis Jan Reineke
11h30 - 12h30	Session **"Frontières et interfaces cyberphysiques"** **Organisateurs**: Patrica D, Antoine F **Orateurs**: Morteza Alavi puis Ayssar Serhan
14h00 - 15h00	**Posters pour les doctorants distanciels wonder.me (https://hackmd.io/eUZ50u-IRISJcqAvAAjhow)**
15h00 - 16h00	Relai de l'intervention de **D. Patterson**, *UC Berkeley*, invité par Alain Tchana, ENS Lyon. https://bbb.wsweet.cloud/b/ala-3oz-xrq-h3s (https://bbb.wsweet.cloud/b/ala-3oz-xrq-h3s)
16h00 - 17h00	**Posters pour les doctorants distanciels wonder.me (https://hackmd.io/eUZ50u-IRISJcqAvAAjhow)**

Journée du Mercredi 09 Juin 2021

Présentiel et distanciel, Webinaire Zoom

Heures	Programme
08h00 - 08h45	Bienvenue, remise des badges et café
08h45 - 09h15	Ouverture et organisation du présentiel
09h15 - 10h15	Session **"Sécurité et intégrité des systèmes,"** **Organisateurs**: Lilian B, Emmanuel B **Orateurs**: Aymen Ladhar puis Annelie Heuser
10h30 - 11h30	Session **"Objets connectés"** **Organisateurs**: *Olivier R, Daniel C* **Orateurs**: Vincent Nougier puis Franck Multon
11h30 - 12h30	**Poster présentiels** **(https://hackmd.io/NcX0rzVuTP6bWSfzukzjQQ#s1)**
12h30 - 14h00	Repas
14h00 - 15h00	Clubs partenaires **Organisateur:** *Bertrand G* Remise du prix du concours RISC V Thales-CNFM-SoC2 **Organisateur**: *Sebastien P*
15h15 - 16h15	Session **"Méthodes et outils"** **Organisateurs**: Kévin M, Mickael D **Orateurs**: John McAllister puis Shuvra Bhattacharyya
16h15 - 17h15	**Poster présentiels** **(https://hackmd.io/NcX0rzVuTP6bWSfzukzjQQ#s2)**

Heures	Programme
19h00 - 23h00	**Social Event** Café des Champs Libres, 10 Cours des Alliés, 35000 Rennes https://www.facebook.com/CafeDesChampsLibres/ (https://www.facebook.com/CafeDesChampsLibres/)

Journée du Jeudi 10 Juin 2021

Présentiel et distanciel, Webinaire Zoom

Heures	Programme
08h30 - 09h15	Bienvenue, café d'accueil
09h15 - 10h15	Session **"Technologie du futur"** **Organisateurs**: *Sébastien LB, Jacques-Olivier K, Jean Michel P* **Orateurs**: Aida Todri-Sanial puis Damien Querlioz
10h30 - 11h30	Session **"IA: Apprentissage et Systèmes Embarqués"** **Organisateurs**: *Gilles S, Maxime P* **Orateurs**: Simon Thorpe puis Benoît Miramond
11h30 - 12h30	**Poster présentiels** **(https://hackmd.io/NcX0rzVuTP6bWSfzukzjQQ#s3)**
12h30 - 13h00	**Session de fermeture**
13h00 - 14h30	Repas

Sessions plénières du GdR SoC 2021

Thème de l'année: SoCs soutenables

Vincent Courboulay, "Le numérique responsable, créateurs de valeurs durables"

⬆️ Back to schedule

Abstract: Dans cette intervention, nous essaierons de mettre en avant la nécessité d'informer, de former et de préparer le futur des sociétés via le développement d'un numérique responsable. Le numérique responsable vise trois enjeux clés : la réduction de l'empreinte (économique, sociale et environnementale) du numérique, la capacité du numérique à réduire l'empreinte (économique, sociale et environnementale) de l'humanité, et la création de valeur durable / innovation responsable via le numérique pour réussir l'e-inclusion de tous. Un numérique responsable est donc un numérique capable de proposer des solutions/innovations soutenables pour la planète, éthiques et inclusives, c'est-à-dire qui respecte et inclut le plus grand nombre car désormais les organisations doivent penser leur organisation non seulement pour être viable économiquement mais aussi en fonction des enjeux sociaux et d'urgence climatique.

Bio: Vincent Courboulay est ingénieur et maître de conférences en informatique à La Rochelle Université depuis 15 ans. Depuis 10 ans il se spécialise dans le numérique responsable (NR) d'abord en créant des formations puis en orientant ses recherches sur cette thématique. Il crée en 2018 l'Institut du Numérique Responsable dont il devient directeur scientifique. Il est à l'origine de la charte, du label et d'un enseignement en ligne accessible à tous qui prennent un rayonnement international dès 2020. Il travaille actuellement sur la notion d'intelligence artificielle responsable et est l'auteur du livre "Vers un Numérique Responsable" paru en 2021 chez Actes Sud.

Caroline Vateau, Directrice BU Numérique Responsable, APL datacenter

⬆️ Back to schedule

Calcul Embarqué Haute Performance

Steven Derrien, "Improving performance and energy efficiency of CNN accelerators through overclocking."

⬆️ Back to schedule

Abstract: Timing speculation, also known as overclocking, is a well-known approach to increase the computational throughput of programmable processors and hardware accelerators. When used aggressively, timing speculation can lead to incorrect/corrupted results due to timing errors.
In this work, we propose a technique to increase the performance and energy efficiency of CNN accelerators through a form of "safe" overclocking thanks to an algorithmic level error detection scheme. This allows our error detection scheme to be expressed directly in C/C++ and then to be implemented on FPGAs using High-Level Synthesis tools. Our prototype on ZC706 demonstrated 68%–77%higher throughput with negligible area overhead.

Bio: Steven Derrien est enseignant-chercheur à l'université de Rennes1 et membre de l'équipe CAIRN (équipe commune INRIA/IRISA). Ses thèmes de recherche portent sur les méthodes et outils pour la conception d'accélérateurs matériels pour FPGAs.

Jan Reineke, "Provably Timing-Predictable Microarchitectures"

⬆️ Back to schedule

Abstract: Microarchitectures are commonly designed without timing predictability in mind. As a consequence, performance-enhancing microarchitectural features in modern processors such as caches and pipelining often result in unpredictability.

In this talk, I will discuss design principles that enable timing predictability without significantly sacrificing performance. In addition, I will report about ongoing efforts to automate formal timing-predictability proofs of HDL designs using SMT solvers.

Bio: Jan Reineke is a professor of computer science at Saarland University. His research centers around problems at the boundary between hardware and software.
In the area of real-time systems, he is particularly interested in principles for the design of timing-predictable hardware and in precise and efficient timing-analysis techniques for multi-core architectures. His recent results include the design of the first provably timing-predictable pipelined processor design

and the first exact analyses for LRU caches.
Another focus of his work are security vulnerabilities of hardware-software systems. Recent results include the development of automatic techniques to detect information leaks introduced by speculative execution, techniques to quantify the information leakage through cache side channels, and automatic methods to obtain highly detailed performance models for modern microarchitectures (uops.info (http://uops.info)).
In 2012, he was selected as an Intel Early Career Faculty Honor Program awardee. He was the PC chair of EMSOFT 2014, a Topic co-chair at DATE 2016, and the PC chair of WCET 2017. His papers have been awarded multiple paper awards, most recently at RTSS 2018 and 2019 and at ECRTS 2017. In 2021, he received an ERC Advanced Grant.

Frontières et interfaces cyberphysiques

Morteza Alavi, "Wideband Bits-in RF-out CMOS Transmitters"

⬆️ Back to schedule

Abstract: : Wireless systems such as WLAN and 5G networks demand low latency and high data throughput.
Moreover, due to employing modulation schemes with a high peak-to-average power ratio, they usually operate at their power back off, degrading their system efficiency. To address these issues, radio-frequency (RF) transmitters (TX) are reinvented and reconfigured as bits-in RF-out architectures, which efficiently convert the input digital baseband data directly into RF signal using advanced CMOS processes. This workshop describes the strengths, possibilities, and challenges of the wideband bits-in RF-out TXs. We will introduce the concept of mixing (RF)-DAC-based TX and stating their advantages and limitations. Subsequently, to address their challenges, such as an efficient operation at power back-off and a clean spectral purity while managing an aggregated bandwidth of more than 300 MHz, we will review some of our recent CMOS-based digital TX prototypes.

Bio: Morteza S. Alavi received his Ph.D. degree in electrical engineering from TU-Delft.
His main areas of research interest are designing RFIC for wireless and cellular

communication systems. He has co-authored Radio-Frequency Digital-to-Analog
Converter (Elsevier, 2016). Since September 2016, he is an assistant professor at TU-Delft. He was the recipient of the Best Student Paper Award (2nd Place) of the 2013 RFIC Symposium. His Ph.D. student also won the Best Student Paper Award (1st Place) of the 2017 RFIC Symposium held in Honolulu, Hawaii, USA.

Ayssar Serhan, "Sub-6GHz SOI-CMOS High-efficiency linear PA architectures: challenges, techniques, and opportunities"

⬆️ Back to schedule

Abstract: High peak-to-average power ratio (PAPR) signals used in LTE and 5G systems require the power amplifier (PA) to be backed-off from its peak power to achieve the necessary system linearity. Linear amplification of high PAPR signals is traditionally achieved by PA operating in back-off where conventional linear PA architectures show poor efficiency. The Doherty PA architecture, which relies on load modulation to improve efficiency in back-off, represents an attractive solution for efficient amplification of high PAPR signals. In this talk, high-efficiency linear SOI-CMOS Doherty PA designed to operate in sub-6GHz bands will be described and recent measurement results will be presented.

Bio: Ayssar Serhan received the M.S. degree and the Ph.D. degree in nanoelectronics and nanotechnologies from the University of Grenoble Alpes (UGA) in Grenoble, France, in 2011 and 2015. In October 2015, he joined the CEA-LETI as RF/mmWave Front-end module design engineer. His research interests include the design of advanced RF PA/FEM architectures (Doherty, Outphasing ...) for WIFI, LTE and 5G applications; the design-for-reliability of CMOS and SOI power amplifiers; the design of tunable RF circuits including power amplifiers and antenna tuners in SOI technologies. He has a strong experience in design-flow development for highly integrated multi-technology RF module simulation.

Sécurité et intégrité des systèmes

Annelie Heuser, "Obfuscation Revealed: Electromagnetic

obfuscated malware classification"

⬆️ Back to schedule

Abstract: In this talk, I will present a novel approach of using side channel information to identify malware threats targetting embedded devices. Using our approach, a malware analyst is able to obtain precise knowledge about malware type and identity, even in the presence of obfuscation techniques that may prevent static or symbolic binary analysis.
Our analysis methodology first preprocesses electromagnetic measurements into the frequency domain and selects relevant frequency bands. We then perform machine learning and deep learning techniques to classify into relevant classes.
In our experiments, we were able to predict three generic malware types (and one benign class) with an accuracy of 99.92%.
Even more, our results show that we are able to classify altered malware samples with unseen obfuscation techniques during the training phase and to determine what kind of obfuscations were applied to the binary, which makes our approach particularly useful for malware analysts.

Bio: Annelie Heuser is CR CNRS IRISA.

Aymen Ladhar, "Concepts dominants dans le domaine du test industriel (et du diagnostic de fautes)"

⬆️ Back to schedule

Abstract: La conception en vue du test, la génération des vecteurs de test et l'ingénierie de test sont devenues des composantes essentielles du flot de conception et de production d'un circuit intégré. Actuellement nous sommes dans l'ère de la nanotechnologie, de 1 micron à la fin des années 80, nous sommes actuellement dans la phase de stabilisation de la 5 nm et des prototypes sont en phase de test en 2 nm. Les avancées technologiques ont eu des répercussions directes sur la testabilité des semi-conducteurs et surtout au niveau du rendement à la fabrication. Concernant la testabilité, les techniques de test ont dû être améliorées et adaptées à travers les outils CAO pour tenir compte des nouveaux types de défauts ainsi la complexité grandissante des systèmes sur puces en termes d'intégration. Par ailleurs, la complexité des nouveaux procédés de fabrication, associée aux nouveaux

phénomènes dont nous venons de parler, introduisent de nouveaux défis :
• Atteindre des niveaux acceptables de rendements le plus rapidement possible
• Maintenir et améliorer ces niveaux de rendements pendant les différentes phases de vie du produit

Dans cette présentation, nous exposons les techniques les plus avancées de test et diagnostic des circuit logiques et utilisées au niveau industriel. Nous présentons aussi les différents défis que nous devons adresser pour assurer la qualité de nos produits.

Bio: Aymen Ladhar is VLSI Test & Yield Engineer at STMicroellectronics

Objets connectés

Vincent Nougier : Directeur GDR Sport et activité physique, Présentation du GDR Sport et activité physique

⬆️ Back to schedule

Franck Multon : Responsable équipe Inria MimeTIC, Les capteurs dans le sport : problématiques et solutions

⬆️ Back to schedule

Méthodes et outils

Shuvra Bhattacharyya, "Simulating Spiking Neural Networks with Timed Dataflow Graphs""

⬆️ Back to schedule

Abstract: This talk presents a novel approach for simulating Spiking Neural Networks (SNNs) that is based on timed dataflow graphs. Whereas conventional SNN simulators compute changes in spiking neuron variables at each time step, the proposed simulation approach focuses on evaluating spike timings. This focus on evaluating when a dataflow actor (spiking neuron) reaches a new spike contributes to making spike evaluation an event-driven computation. The resulting event-driven simulation approach avoids unnecessary computations at time steps that lie between spiking

events. This optimization is achieved while avoiding the large overheads associated with lookup tables that are incurred in existing event-driven approaches. Useful features of the proposed new simulation approach include improved simulation speed, enabled by the event-driven operation; design flexibility in that the simulation is not limited to a specific spiking neuron model or network topology; and retargetability across different hardware platforms and implementation languages, enabled by the rigorous use of dataflow modeling concepts. Our results show identical spiking behavior compared to simulation using a conventional (time-based) simulator while providing significant improvement in execution time.

Bio: Shuvra Bhattacharyya is with University of Maryland and IETR.

John McAllister, "Quantum Circuit Mapping for Nearest-Neighbour Quantum Processors"

⬆️ Back to schedule

Abstract: Quantum computation is an extremely exciting and fast-moving area attracting considerable attention for its potential to unlock computational capabilities well beyond the classical computers available to all of us now. Google have claimed quantum supremacy using their Bristlecone processor, yet the field has very far to go before useful quantum computing is a widespread reality. The quantum processors which power these computers use locally-connected qubits, meaning two qubits need to be physically connected to be combined via a quantum gate. Swap gates are inserted into the quantum circuits used to describe the quantum program when this is not the case. Minimising the number of swaps is not only a performance concern – longer circuits take more time to complete - but also an issue of reliability, since if circuits take too long to execute, current quantum processors can't produce reliable results. Minimising swap cost is currently a compile-time problem the complexity of which scales dramatically with the number of qubits and the length of the circuit. This presentation will discuss techniques to significantly reduce either the swap cost, or the compile-time analysis complexity, or a combination of both.

Bio: John McAllister is with Queen's University, Belfast.

Technologies du futur

Damien Querlioz, "Memory-Centric Artificial Intelligence"

⬆️ Back to schedule

Abstract: When performing artificial intelligence tasks, central and graphics processing units consume considerably more energy for moving data between logic and memory units than for doing actual arithmetic. Brains, by contrast, achieve superior energy efficiency by fusing logic and memory entirely, performing a form of “in-memory” computing. Currently emerging memory nanodevices such as (mem)resistive, phase change, and magnetic memories give us an opportunity to achieve similar tight integration between logic and memory. In this talk, we will look at neuroscience inspiration to extract lessons on the design of in-memory computing systems. We will first study the reliance of brains on approximate memory strategies, which can be reproduced for artificial intelligence. We will give the example of a hardware binarized neural network relying on resistive memory. Binarized neural networks are a class of deep neural networks discovered in 2016, which can achieve state-of-the-art performance with a highly reduced memory and logic footprint with regards to conventional artificial intelligence approaches. Based on measurements on a hybrid CMOS and resistive hafnium oxide memory chip exploiting a differential approach, we will see that such systems can exploit the properties of emerging memories without the need for error-correcting codes, and achieve extremely high energy efficiency. Then, we will present a second approach where the probabilistic nature of emerging memories, instead of being mitigated, can be fully exploited to implement a type of probabilistic learning. We show that the inherent variability in hafnium oxide memristors can naturally implement the sampling step in the Metropolis-Hastings Markov Chain Monte Carlo algorithm, and train experimentally an array of 16,384 memristors to recognize images of cancerous tissues using this technique. These results highlight the interest in understanding and embracing the unreliable nature of emerging devices in artificial intelligence designs.

Bio: Damien Querlioz is a CNRS Researcher at the Centre de Nanosciences et de Nanotechnologies of Université Paris-Saclay. His research focuses on

novel usages of emerging non-volatile memory and other nanodevices, in particular relying on inspirations from biology and machine learning. He received his predoctoral education at Ecole Normale Supérieure, Paris and his PhD from Université Paris-Sud in 2009. Before his appointment at CNRS, he was a Postdoctoral Scholar at Stanford University and at the Commissariat a l'Energie Atomique. Damien Querlioz is the coordinator of the interdisciplinary INTEGNANO research group, with colleagues working on all aspects of nanodevice physics and technology, from materials to systems. He is a member of the bureau of the French Biocomp research network. He has co-authored one book, nine book chapters, more than 100 journal articles, and conference proceedings, and given more than 50 invited talks at national and international workshops and conferences. In 2016, he was the recipient of an ERC Starting Grant to develop the concept of natively intelligent memory. In 2017, he received the CNRS Bronze medal. He has also been a co-recipient of the 2017 IEEE Guillemin-Cauer Best Paper Award and of the 2018 IEEE Biomedical Circuits and Systems Best Paper Award.

Aida Todri-Sanial, "Neuromorphic Computing with Oscillatory Neural Networks"

⬆️ Back to schedule

Abstract: Current classical computers are playing a critical role in advanced research such as in biology, climate analysis, economics, genomics, finance, etc. In many aspects, computing fuels the advances of our modern society. Yet, recent developments in artificial intelligence (AI) and machine learning will require even more powerful computing systems such as exascale computations per second due to an ever-increasing amount of data. But classical computing systems are hindered by the von-Neumann communication bottleneck, the physical separation between processor and memory. This offers the opportunity to explore a novel computing paradigm where the brain can serve as a computational model of how to deal with large amounts of (often fuzzy) information while being extremely dense, error-resilient and power efficient. A novel and alternative neuromorphic computing paradigm based on oscillating neural networks (ONN) will be presented in this talk. Energy efficient relaxation oscillators based on phase-change material for oscillating neurons and tunable memristors for synapses are the

building blocks of ONN architecture. Inspired by neural oscillations or brain waves, in ONN, the information is encoded in the phase of coupled oscillators. The talk will cover aspects from materials, devices, circuits to ONN architecture design and hardware implementation and demonstration on AI tasks. This work is conducted in the framework of the EU H2020 NEURONN project, www.neuronn.eu (http://www.neuronn.eu)

Bio: Dr. Aida Todri-Sanial is a CNRS Research Director at LIRMM lab and a Senior Member of IEEE. Dr. Todri-Sanial was a visiting fellow at the Cambridge Graphene Center and Wolfson College at the University of Cambridge, UK, during 2016-2017. Previously, she was an R&D Engineer for Fermi National Accelerator Laboratory, IL. She has also held visiting research positions at Mentor Graphics, Cadence Design Systems, STMicroelectronics, and IBM TJ Watson Research Center. Her research interests focus on emerging technologies and novel computing paradigms such as neuromorphic and quantum computing. She has co-authored more than 100 publications on high-impact journals and conferences. Dr. Todri-Sanial was a recipient of John Bardeen Fellow in Engineering in 2009, CNRS Prime d'Excellence Scientifique in 2012, ACM Distinguished Speakers 2016-2018, CNRS Bronze Medal in 2016, and ACM SIGDA Meritorious Service Award in 2020. Dr. Todri-Sanial is the EU H2020 NeurONN project coordinator and a participant in the EU H2020 SmartVista and EU H2020 CONNECT projects. Website: https://www.lirmm.fr/aida-todri-sanial (https://www.lirmm.fr/aida-todri-sanial)

Intelligence artificielle et systèmes embarqués

Simon Thorpe - "Pourquoi utiliser des Spikes ?""

⬆️ Back to schedule

Les systèmes de Deep Learning constituent aujourd'hui l'état de l'art pour de nombreux problèmes, notamment le traitement des images et du son. Bien que ces systèmes soient superficiellement similaires aux réseaux neuronaux biologiques, il leur manque généralement l'une des caractéristiques clés des neurones biologiques - l'utilisation de spikes. Dans cette présentation, je soutiendrai qu'il existe de nombreuses raisons pour lesquelles les futurs systèmes devront presque certainement utiliser des spikes. Il s'agit notamment de l'efficacité énergétique de l'utilisation de réseaux de spikes

épars, qui pourrait être particulièrement importante pour les systèmes embarqués. Mais les spikes permettent également le développement de schémas d'apprentissage non supervisés qui sont beaucoup plus plausibles que l'apprentissage basé sur la rétropropagation d'erreurs utilisé dans les réseaux neuronaux conventionnels.

Benoît Miramond, "Vers une approche bio-inspirée de l'IA embarquée.""

⬆️ Back to schedule

Abstract: La diffusion massive de l'IA repose essentiellement aujourd'hui sur l'utilisation de ressources de calcul dans le cloud, masquant ainsi l'incroyable consommation énergétique de ces algorithmes. L'ouverture de l'IA vers des contextes plus embarqués (AI at the Edge) révèle le défi qui attend ses acteurs et ouvre par la même occasion un nouveau terrain applicatif très compétitif sur lequel aucun monopole n'existe encore et où beaucoup reste encore à faire tant par les ingénieurs que par les chercheurs. En accédant à ce stade de déploiement de l'IA, différents niveaux de complexité s'accumulent. Au delà de la complexité habituelle d'apprentissage des méthodes de Machine Learning, la dimension embarquée apporte aussi des contraintes nouvelles en terme d'empreinte mémoire, de débit de données, de latence et ben évidemment de consommation énergétique et/ou de dissipation thermique.
Nous nous intéresserons dans cet exposé uniquement aux approches par réseaux de neurones artificiels pour lesquelles plusieurs solutions de compression se bousculent déjà pour plusieurs types de cibles matérielles. Mais le groupe eBRAIN du laboratoire LEAT se différencie par une approche inspirée de la biologie et plus précisément de la formidable efficacité de cerveau pour définir des modèles et des architectures neuromorphiques plus économes pour l'embarqué.
Des modèles convolutionnels aux réseaux de neurones à spikes en passant par les cartes auto-organisatrices, plusieurs modèles de réseaux et d'apprentissage seront présentés ainsi que leurs résultats dans des contextes applicatifs diverses comme l'IoT, l'automotive la robotique ou bien le spatial.