6th national RISC-V student contest 2025-2026

Sponsored by Thales, the GDR SOC² and the CNFM

Accelerating an FFT on CVA6 RISC-V processor

You are students and like new challenges.
You are interested in electronics and computer architectures. You want to participate in the adventure of a renowned OpenHW processor core.
Then join this contest and win up to € 5,000!

Introduction

Thales is a world leader for mission critical information systems for the security, defense, space and aerospace domains. It employs about 83,000 people in 68 countries. Following the success of the five previous national RISC-V student contests from 2020 to 2025, Thales, together with the **GDR SOC²** and the **CNFM**, are proud to announce the 6th edition of the contest (2025-2026).

This year's contest will focus on **architectural modifications** of the **CV32A6** RISC-V soft-core to accelerate a **Fast Fourier Transform (FFT)** algorithm processing 2^n samples[1].

RISC-V is a recent open ISA that is gaining every day more attraction. From this ISA, ETH Zürich has designed a mid-range open-source application core named **ARIANE**. It has the capacity to execute rich operating systems and integrates an MMU function and several privilege levels. In 2019, the OpenHW Group (now **OpenHW Foundation**) was created with the ambition to design industrial-grade RISC-V processor core IPs. OpenHW has integrated the ARIANE core as its new 64-bit application core under the name CV64A6. Thales engineers have created a more compact 32-bit version from the original design, named **CV32A6**. CV32A6 and CV64A6 share the same source code and are together referred to as CVA6.

Targeted participants

You are a team of students:

[1] The integer *n* will be decided before the kit is released to have a decent simulation time.

- 1 to 4 **Master 2 students** (or equivalent: final year in engineering schools)
- All registered in a **French engineering school or university**
- Coached by one or several **supervisors** (teachers, assistant professors, professors). PhD students can additionally join as supervisors.

Although the contest does not primarily target Master 1 students, they are also welcome.

You have the following skills or will get some or all of them:

- Digital electronics
- HDL languages
- Digital simulation
- Computing architecture
- Embedded programming
- FPGA design and tools

Although this year's contest is about FFT, digital signal processing skills are not needed to join, as the work will be about computing architecture to optimize an application written in C. The specific maths will be addressed before by the organizers, when they prepare the kit.

The broad timeline of the contest should make it a good fit for your last-year academic project. You can start a few months after the official kick-off date or submit results weeks or months before the deadline, e.g. before you start an internship.

Description of the contest

Inputs

The organizers will prepare a kit composed of:

- A testbench to simulate the CV32A6 in its RTL form;
- The parameters of the CV32A6 core to consider;
- Scripts for synthesis of the baseline core;
- A BSP;
- A reference design to run the CV32A6 core on a FPGA development board;
- The FFT application to accelerate, written in C, and reference patterns;
- The CoreMark[2] application running in bare metal on the processor core;
- The MNIST application running in bare metal on the processor core (generated by generated by Aidge, an open source platform co-developed by Thales, CEA and other organizations).

The kit will be available on a Thales GitHub repository.

You will get support from your university/school and coaching from your supervisor. The organizers will remain in contact with the teams and the supervisors.

Communication and support

Supervisors will provide level 1 support to the team. Level 2 support[3] will be addressed to the contest organizers and may only be exercised if the issue cannot be solved at level 1.

A Discord server will be created by the organizers to:

- Communicate announcements and practical information;
- Allow level 2 support;
- Host forums and discussions open to all participants.

[2] This year, the MNIST and CoreMark applications will be used for non-regression.

[3] Level 2 support mostly includes issues with the delivered kit and clarifications about eligible optimizations. Level 2 support does not debug the teams' solutions.

The Discord server will log messages so that teams, which will start later, can recover past information. No mailing list will be maintained; all messages will go through Discord after the team is registered. The invitations to the Discord server will be sent when the registration is accepted.

The French language will be used on Discord and during the interim event (English can be used by foreign students). Results can be reported in French or English.

Prerequisites

Most parts of the CVA6 processor are written in **SystemVerilog**, a language widely adopted by the industry. You will have to use this language to modify the core.

The list of CAD tools and the FPGA board are unchanged w.r.t. the previous editions, so that schools/universities having already participated may have the pre-requisite for this contest.

The **FPGA development board** selected for this context is the Digilent Zybo Z7-20[4]. The list of necessary material is:

Reference	URL	Remark
Zybo Z7-20	https://store.digilentinc.com/zybo-z7-zynq-7000-arm-fpga-soc-development-board/	Zybo Z7-10 is too small for CVA6.
Pmod USBUART	https://store.digilentinc.com/pmod-usbuart-usb-to-uart-interface/	Used for the console output
JTAG-HS2 Programming Cable	https://store.digilentinc.com/jtag-hs2-programming-cable/	
Connectors	https://store.digilentinc.com/pmod-cable-kit-2x6-pin-and-2x6-pin-to-dual-6-pin-pmod-splitter-cable/	At least a 6-pin connector Pmod is necessary; other references may offer it.

Supervisors must **ensure that student teams will have this FPGA environment**. They can order the complete set from CNFM (contact: fpga@cnfm.fr).

The Siemens EDA **Questa** digital simulator will be needed to test your solutions and will be supported by Thales[5]. Questa licenses can be obtained through CNFM. As the Questa licence tokens are hosted on a CNFM server, you will likely need support from your IT (e.g. configure a firewall, communicate IP addresses with CNFM…).

AMD Xilinx Vivado will be used for the synthesis and place & route to port CV32A6 to the FPGA board. Participants can use evaluation licenses or the AMD University Program.

The kit prepared by Thales will run on Linux Ubuntu 20.04. You can use other host OSes, but you will not receive IT support by the organizers.

CAD tools are available in schools/universities through CNFM. For any information, supervisors can get in touch with cao@cnfm.fr.

From previous years' experience, you should **anticipate as soon as possible the provisioning of CAD licences and FPGA board, and the setup of the IT infrastructure** to avoid delays.

Work to perform and constraints

Your goal is to modify the CV32A6 architecture and/or add a coprocessor to accelerate the FFT algorithm provided as an application written in C. The results computed by your solution shall match the reference patterns, on a per-bit basis.

Your creativity should prevail as long as the following constraints are fulfilled:

- Your solution must mainly rely on the CV32A6 processor or in a tightly-coupled coprocessor attached to the CV-X-IF interface (not on a "coarse grain" accelerator)[6].

[4] No other FPGA boards will be accepted as the jury will replay results on its board.
[5] Teams can use other simulators, e.g. Verilator, to develop their solution, but won't receive support on these tools.
[6] We do not want to see a hard-wired accelerator that computes the full FFT (or partial FFT of 8 or more points). You can also modify CVA6 internal architecture beyond modifications related to the math computation.

- You cannot increase the total memory size of data caches.
- You cannot increase the total memory size of instruction caches.
- You cannot decrease the CV32A6 operational frequency more than 20% (as measured by Vivado timing analysis)
- You can alter the source code of the FFT C code to exploit your architectural evolutions, e.g. to express parallelism, to interface with a coprocessor, to address custom instructions, to reorder operations…
- To be confirmed: You cannot replace the sine and cosine (= complex exponential) computation by a pre-computed table.
- You can modify the compiler and SW environment to recognize your specific instructions or you can use inline assembly in the C code. Other modifications of the software environment (e.g. changing the compiler optimization options) will not be considered.
- Your solution shall keep the compatibility with the RV32IM_Zicsr instruction set (but you can add ISA extensions).
- For non-regression, your solution shall run the CoreMark and MNIST applications on the FPGA board[7].
- The size of your hardware design fits in the FPGA of the Zybo Z7-20 board.
- You cannot replace the CV32A6 by another core, but you can deeply modify CV32A6. You cannot use CV64A6.
- You can use existing open-source code, as long as you respect its licence terms and the compatibility with the Apache/Solderpad licence[8].

The organizers cannot anticipate all teams' ideas. If you have a doubt about your solution eligibility, share with the organizers a detailed description of your planned solution to get a pre-approval. Discussions will never be shared with other teams.

Outputs

You shall provide:

- A 6-page report presented as a scientific paper, in French or English, with illustrations[9]
- A 10-minute recorded video, that will be presented during the defense session (and during the prize ceremony for the winning teams), in French or English
- A link to your new source code and results uploaded on GitHub (under Apache or Solderpad licenses)
- The reports from the tools that justify the results presented in the report.

During the course of the contest, the organizers will provide additional instructions or clarifications. A standardized way to report results, according to the defined criteria, will also be provided.

Contributions to the OpenHW Foundation

Thales may integrate some contributions (or derivatives) in OpenHW repositories, mentioning the students' names. The OpenHW Foundation criteria for accepting contributions differ from those used in this contest.

Prizes and jury's criteria

To be eligible for the final selection, your solution must simulate correctly, work on the FPGA board with the environment provided in the kit, provide the expected results (on a per-bit basis) and fulfill the constraints listed above.

The jury will then rank the results based on the number of cycles needed to compute the FFT in simulation.

[7] CoreMark and MNIST will be compiled for the RV32IM_Zicsr extensions. CoreMark scores are ignored in this year's contest. MNIST shall provide the same results as with the reference kit.
[8] This means for instance that you shall not include GPL or LGPL code.
[9] An IEEE template is recommended: https://www.ieee.org/conferences/publishing/templates.html.

If there are ties, i.e. teams with a close number of cycles (<1%), the results will be separated with the maximum frequency (as measured with Vivado timing analysis). If the tie persists when comparing frequencies (<1%), the FPGA resources will be considered[10].

The jury will replay the finalists' results in its environment to avoid any differences due to local configurations.

The jury will be sovereign with consider specific situations (if not clearly defined in the rules) while maintaining the fairness between teams.

Thales will award **€ 5,000** to the winning team and **€ 3,000** to the second best team (for teams between 2 and 4 participants). Prizes[11] will be equally shared among the team members. If an awarded team only has 1 participant, the individual will get € 2,500 for the first prize and € 1,500 for the second prize.

The winning teams will present their video at an event organized by Thales and/or the GDR SOC². In addition to the prize, they will get a diploma.

Registration

Teams may register anytime until **28th February 2026** and run the contest at their own pace. They will recover past information from the Discord server.

Teams from a same university/school will register separately and can start at different dates.

Teams may deliver their results at any time before the end of the contest on **May 4th, 2026**.

To register, the supervisor will send an email to Jérôme Quévremont, Sébastien Pillement and Pascal Benoit (addresses below) with the following details:

- Name of the university/school
- Name of the team[12]
- Supervisor(s): Name, position (e.g. assistant professor), email address
- For each student: Name, option/major/"filière", Master 1 / Master 2, email address

The organizers will then check whether the registration is valid and send Discord time-limited invitations to the students and the supervisors.

A few additional rules:

- Teams without a supervisor are not accepted.
- If you are more than 4 students, register as several teams.
- There may be several teams from a given university/school.
- A team may include students from different options/majors/"filières".
- A student may not be in more than one team.
- A supervisor may supervise several teams and ensure no co-operation between these teams on their technical solutions. Joint teaching/learning (e.g. SystemVerilog, ISA, architecture courses) is accepted and encouraged.
- The supervisor(s), including PhD students if any, have an educational role (teaching, coaching, supporting…) and shall not design the team's solutions.
- The supervisor(s) may be replaced during the project.
- Once the team is registered, the list of students shall not change (except under exceptional circumstances, with the organizers' agreement).

[10] Of course, we target the smallest number of cycles, the highest frequency and the smallest use of resources (number of FFs + LUTs excluding LUTRAM).

[11] The prizes will be provided as prepaid Mastercard cards a few months after the prize ceremony (because of administrative delays). Award-winning team members will have to provide personal details needed by the payment organization.

[12] It is important if there are several teams from a same university/school. If only one team registers, it can have the name of its university/school. The team name will be printed on the winners' diploma.

- The organizers will consider specific situations (if not clearly defined in the rules) while maintaining the fairness with other teams.

Abbreviations

BSP	Board Support Package
CAD	Computer-Aided Design
CNFM	Coordination Nationale pour la Formation en Micro-électronique et en nanotechnologies
FF	Flip Flop
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
GDR	Groupe de Recherche
HDL	Hardware Description Language
IP	Intellectual Property
IT	Information Technology
ISA	Instruction Set Architecture
LUT	Look-Up Table
MMU	Memory Management Unit
MNIST	Modified National Institute of Standards and Technology database
RAM	Random Access Memory
RISC	Reduction Instruction Set Computer
RTL	Register Transfer Level
SoC	System on Chip

Planning

	Thales	GDR SOC²	CNFM	Teams and universities/schools
1st October 2025	Launch of the contest			You can start registering teams. You can anticipate the contest by gaining knowledge on the CV32A6, SystemVerilog, reusing previous years' repositories… **You should anticipate the provision of tools and the FPGA board (see above).** No support from the organizers is offered until the kit is delivered.
October 2025	Delivery of the kit as a GitHub repo.			The teams can start later than this date.
October 2025 to April 20st, 2026	Level 2 support (fix bugs in the kits…) The support will end two weeks before the submission deadline.			Run the project. Supervisors provide level 1 support to the student team.
January/February 2026	Organization of an online event: teams' introduction, guidelines to prepare submission, Q&A…			Participation to the event
February 28th, 2026				Deadline to register teams
May 4th, 2026 at 23:59				**Deadline to submit results in a GitHub repository (reports, source code…)**. The teams can submit results sooner. The defense videos will have to be provided a few days after.
Mid/end of May 2026 (TBA)	Organize the online defense session as online meeting(s)			Attend the online defense session: recorded video (10') + live Q&A (5')

	Thales	GDR SOC²	CNFM	Teams and universities/schools
June 17th-19th, 2026	Final event at Colloque GDR SOC² in Marseille: prize announcement, presentation by the winning teams (recorded videos).			You are welcome to receive the diploma and congratulations.

Contacts

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CNFM	Pascal Benoit	pascal.benoitⓐlirmm.fr

History

Date	Version	Comment
2025-06-xx	v0.x	Drafts in progress
2025-07-01	V1.0	Version for review by organization team
2025-07-04	V1.1	First public version; a “to be confirmed” to address when the contest starts.
2025-08-26	V1.2	Updated date for the final event.